UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,733	01/22/2004	Peter John McElheny	A1167	7320

45851 7590 12/29/2005

G. VICTOR TREYZ
FLOOD BUILDING
870 MARKET STREET, SUITE 984
SAN FRANCISCO, CA 94102

EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,733	MCELHENY, PETER JOHN	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☐ accepted or b)☒ objected to by the ~~Examiner~~ draftsperson.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Application and IDS filed on 1/22/2004. Claims 1-21 are pending.

Drawings

2. The drawings filed on 1/22/2004 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Objections

3. **Claims 1-6,18-21** are objected to because of the following informalities:

As per **claim 1**, --into-- should be inserted before "account" (line 8) for proper grammar and for greater clarification.

As per **claim 3**, --into-- should be inserted before "account" (line 5) for proper grammar and for greater clarification.

As per **claim 4**, "the amounts that the signals" (line 8) should be --amounts of the signals that-- for proper antecedent basis and for greater clarification.

As per **claims 2-6**, the claims are also objected to for incorporating the above error into the claim by claim dependency.

As per **claim 18**, "the logic" (line 2) should be --a logic-- for proper antecedent basis; "the expected" (line 3) should be --an expected-- for proper antecedent basis.

As per **claim 19**, --,-- (coma) should be inserted after "high" (line 4) for further clarification. The claim is also objected to for incorporating the above error into the claim by claim dependency.

As per **claim 20**, "the logic" (line 3) should be --a logic-- for proper antecedent basis.

As per **claim 21**, --into-- should be inserted before "account" (line 5) for proper grammar and for greater clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-2,5,7,9,13,21** are rejected under 35 U.S.C. 102(e) as being anticipated by **Hart et al.** (U.S. Patent Application No. 2004/0216074).

As per **claims 1,7,21**, the elements of the claims are illustrated in Fig. 7, wherein the desired logic design (i.e., the user circuit) being specified, created or received is further described in paragraphs [0060]-[0061] for which the evaluation step 701 is

applied, wherein the configuration data generated/produced at 703 enabling well biasing of transistors for implementing in the programmable logic device includes taking into account of power consumption due to gate leakage effects as part of the routing as further described in paragraphs [0014]-[0016], [0025]; wherein the computer readable medium, computing equipment, instructions are part of the computer implemented method as described in paragraph [0091], being necessary to carry out the computer-implemented method.

As per **claims 2,5,13,** all of the elements of claims 1,7, from which the respective claims depend, are discussed in the rejections of claims 1 and 7 above, wherein the further limitation in which the type of signals information being gathered either from the logic designer and/or generated automatically is also part of the critical path designation or extraction described in paragraph [0061], wherein the type of signals or signals information correspond to the speed of the circuit paths (i.e., critical or non-critical).

As per **claim 9**, all of the elements of claim 7, from which the claim depends, are discussed in the rejection of claim 7 above, wherein the plurality of logic design constraints are at least the critical path, timing (i.e., delays) and power leakage reduction constraints as described in paragraphs [0063]-[0064], which are balanced as further described in paragraphs [0073].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 3-4,6,8,10-12,14-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hart et al.** (U.S. Patent Application No. 2004/0216074) in view of **Rafik S. Guindi et al.** ("Design Techniques for Gate-Leakage Reduction in CMOS Circuits", 2003 IEEE, pp. 61-65).

As per **claims 3-4,6,8,10**, **Hart et al.** disclose all of the elements of claims 1,7, from which the respective claims depend, as discussed in the rejections of claims 1 and 7 above. However, **Hart et al.** failed to teach the leakage effects by taking into account of transistor stacking effects, including the particular positions within the stacks based on signals that are expected or likely to be high or low. **Rafik S. Guindi et al.** disclose design techniques for gate-leakage reduction in CMOS circuits which include taking into account of transistor stacking effects, including the particular positions within the stacks based on signals that are expected or likely (i.e., probability) to be high or low (see especially sections 5, 3.2 and 4.1; abstract). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the design techniques for gate-leakage reduction of **Rafik S. Guindi et al.** into the method/system of **Hart et al.** because such incorporation would further reduce power consumption of the logic design being implemented on the programmable logic devices as intended by **Hart et al.** by further taking into consideration the signals probability and transistor stacking effects as further taught by **Rafik S. Guindi et al.**.

As per **claims 11-12, Hart et al.** in view of **Rafik S. Guindi et al.** disclose all of the elements of claim 10, from which the claims depend, as discussed above, wherein the information which includes information that the first signal is high more often than the second signal is further taught by **Rafik S. Guindi et al.** as part of the importance of signal probability (i.e., the first signal being high more often than the second signal) being used to determine the particular positions or configurations or assignments of the transistors being selected (see section 5, items 4 and 5). However, **Hart et al.** failed to specifically include such information being received or produced, for generating the data configuration for the programmable logic devices. It would have been further obvious to one of ordinary skilled in the art at the time of the invention to adapt the system/method of **Hart et al.** to include such information as being received or produced because such information is vital to the gate-leakage reduction as taught by **Rafik S. Guindi et al.** and such user designation and/or automatic generation are also supported by the system/method of **Hart et al.** (see paragraph [0061]).

As per **claims 14,17-20**, **Hart et al.** teaches the configuration data generation/production to reduce power consumption due to gate leakage, including receiving the logic design as discussed in the rejections of claims 1,7,21 above and including the use of placement and routing tools (see paragraphs [0063]-[0064]. However, **Hart et al.** failed to specifically teach the routing/configuration of the programmable logic device based on the likelihood of the signals being high or low to reduce power consumption due to gate leakage, including ensuring that at least some or a fraction of the signals that have a high likelihood of being high are routed to those

transistors that are more likely to produce the lower gate leakage than the other transistors when high voltages are applied to their gates. **Rafik S. Guindi et al.** disclose design techniques for gate-leakage reduction in CMOS circuits which include taking into account of transistor stacking effects, including the particular positions within the stacks (i.e., at least some or a fraction of the signals that have a high likelihood of being high are routed to those transistors that are more likely to produce the lower gate leakage than the other transistors when high voltages are applied to their gates) based on signals that are expected or likely (i.e., probability) to be high or low (see especially sections 5, 3.2 and 4.1; abstract). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the design techniques for gate-leakage reduction of **Rafik S. Guindi et al.** into the method/system of **Hart et al.** because such incorporation would further reduce power consumption of the logic design being implemented on the programmable logic devices as intended by **Hart et al.** by further taking into consideration the signals probability and transistor stacking effects as further taught by **Rafik S. Guindi et al.**.

As per **claim 15**, **Hart et al.** in view of **Rafik S. Guindi et al.** teaches all of the elements of claim 14, from which the claim depends, wherein the constraints including a minimum desired clock speed to be satisfied whiled reducing the power consumption due to gate leakage is also taught by **Hart et al.** as part of the timing information constraints being received (see paragraphs [0062]-[0063],[0067]).

As per **claim 16**, **Hart et al.** in view of **Rafik S. Guindi et al.** teaches all of the elements of claim 14, from which the claim depends, wherein the logic synthesis and optimization are part of the mapping and placement as described in paragraph [0058].

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action. In particular the following prior arts made of record are most relevant:

U.S. Patent Nos.:

6,324,678, especially col. 36, line 35 to col. 40, line 16; Figs. 2-4;

6,038,386, especially col. 2, line 39 to col. 3, line 3;

5,712,790, especially col. 2, line 56 to col. 3, line 12;

6,345,379, especially col. 17, lines 53-67; col. 10, line 15 to col. 11, lie 25; col. 13, lines 21-31.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
December 24, 2005